REMARKS

Claims 2, 5-9, 25-43, and 45-56 are pending in the present application. By the present amendment, claims 5, 8, 25, 27, 29, 31, 33-39, and 41-43 have been amended. Claims 1, 3, 4, 10-24, and 44 have been canceled. New claims 54-62 have been introduced. New claims 58-62 depend from elected claims but should be withdrawn from consideration as be directed to a non-elected species. The present application, as amended, includes six independent claims - 2, 5, 6, 7, 8, and 57.

Independent claim 2 recites a multiple die semiconductor assembly comprising first and second semiconductor dice, an intermediate substrate positioned between the dice, and at least one decoupling capacitor, where "a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of" the first or second semiconductor die or a topographic contact conductively coupled to the first or second semiconductor die. Claim 2 has been rejected under 35 U.S.C. §103 in view of Venkateshwaran et al. (US 6,388,336) and Suzuki et al. (US 5,532,910).

According to the Office Action, although the Venkateshwaran et al. reference "does not disclose at least one decoupling capacitor ... wherein a thickness dimension of said decoupling capacitor is accommodated" as recited in claim 2, it would have been obvious to provide such a capacitor in the Venkateshwaran et al. structure because "Suzuki et al. utilizes a decoupling capacitor accommodated in a space." However, applicants note that claim 2 does not merely recite that the decoupling capacitor is "accommodated in a space." Rather, claim 2 recites that a thickness dimension of the decoupling capacitor is accommodated in a space defined by a thickness dimension of the first or second semiconductor die or a topographic contact conductively coupled to the first or second semiconductor die. Neither the Suzuki et al. reference nor the Venkateshwaran et al. reference provide any teaching or suggestion in this regard. All one of ordinary skill could reasonably be expected to glean from the combination of these two references is that it might be beneficial to provide a decoupling capacitor in some part

of the structure of Venkateshwaran et al.* Neither reference provides any guidance suggesting that the thickness dimension of the decoupling capacitor be accommodated in a space defined by a thickness dimension of the first or second semiconductor die or a topographic contact conductively coupled to the first or second semiconductor die. Accordingly, *prima facie* obviousness has not been established by the combination of the Venkateshwaran et al. and Suzuki et al. references.

New independent claim 57 is similar in scope to claim 2 except it further limits the "accommodation" recitation to that where the thickness dimension of the decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to the first or second semiconductor die. The topographic contacts of the Venkateshwaran et al. reference are poorly suited to accommodate anything of significant thickness, let alone a decoupling capacitor.

Independent claims 6 and 7 are also similar in scope to claim 2 in that they each recite a multiple die semiconductor assembly including a decoupling capacitor wherein the decoupling capacitor is accommodated in a space defined by a thickness dimension of the first or second semiconductor die or a topographic contact conductively coupled to the first or second semiconductor die. Claim 6 has been rejected under 35 U.S.C. §103 in view of the same references applied to claim 2. Accordingly, applicants respectfully assert that *prima facie* obviousness has also not been established with respect to claim 6, for the reasons set forth above in the discussion of claim 2. Claim 7 has been rejected under 35 U.S.C. §103 in view of Hur (US 6,646,334) and Suzuki et al.. However, the replacement of the Hur reference for the Venkateshwaran et al. reference still fails to remedy the deficiency noted above in the discussion of claim 2, i.e., nothing in the Hur reference provides any teaching or suggestion that the thickness dimension of the decoupling capacitor be accommodated in a space defined by a thickness dimension of the first or second semiconductor die or a topographic contact conductively coupled to the first or second semiconductor die.

* This statement is made for the purposes of illustration only and should not be taken as an admission by applicants that it would have been obvious to provide a decoupling capacitor in some part of the structure of Venkateshwaran et al.

Independent claim 8 recites a multiple die semiconductor assembly comprising first and second semiconductor dice and an intermediate substrate positioned between active surfaces of the dice. The first die is electrically coupled to the intermediate substrate by topographic contacts extending from the active surface of the first die to the first surface of the intermediate substrate. Similarly, the second die is electrically coupled to the intermediate substrate by topographic contacts extending from the active surface of the second die to the second surface of said intermediate substrate. In an effort to clarify the distinction between a conductive wire (see, e.g., ref. #56 of Hsuan et al.) or an electrical lead (see, e.g., ref. #42a of Venkateshwaran et al.) and an intermediate substrate (see, e.g., ref. #40 of the present application), claim 8 has been amended to further recite that the intermediate substrate "includes a network of conductive contacts formed thereon." Claim 8 has been rejected under 35 U.S.C. §102(e) in view of Akram (US 6,300,163), Hsuan et al. (US 6,236,109), and Venkateshwaran et al. (US 6,388,336).

Regarding the citation of the Akram reference under 35 U.S.C. §102(e), applicants note that not all of the elements of claim 8 are disclosed in the Akram reference. Specifically, the Akram reference merely suggests the use of topographic contacts between one of the dice and one side of the printed circuit board. The Akram reference fails to teach provision of topographic contacts on both sides of the printed circuit board between the respective dice. Accordingly, the §102(e) rejection of claim 8 citing the Akram reference is unsupported by the art and should be withdrawn.

Regarding the citation of the Hsuan et al. reference under 35 U.S.C. §102(e), applicants note that not all of the elements of claim 8 are disclosed in the Hsuan et al. reference. Specifically, the Hsuan et al. reference fails to teach provision of an intermediate substrate including "a network of conductive contacts formed thereon." Rather, Hsuan et al. merely show a conductive wire 56 between two stacked chips 50, 52 (see Fig. 3). The use of the Venkateshwaran et al. reference is similarly deficient in that it merely shows conductive leads 42a interposed between two chips 41a, 45a. Accordingly, the §102(e) rejections of claim 8 citing the Hsuan et al. and Venkateshwaran et al. references are unsupported by the art and should be withdrawn.

Independent claim 5 is similar in scope to claim 8 except it further recites an "additional substrate" including "a network of conductive contacts formed thereon." Claim 5 has been rejected under 35 U.S.C. §102(e) in view of Hur (US 6,646,334); however, as is the case with the Hsuan et al. and Venkateshwaran et al. references cited above, the Hur reference fails to teach provision of an intermediate substrate including "a network of conductive contacts formed thereon." Rather, the Hur reference merely shows conductive leads interposed between respective chips. Accordingly, the §102(e) rejection of claim 5 citing the Hur reference is unsupported by the art and should be withdrawn.

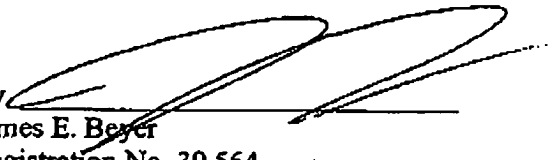
Applicants note that each of the remaining claims presently pending in the application depend directly or indirectly from each of the above-noted independent claims and, as such, are in condition for allowance for the reasons discussed above.

CONCLUSION

Applicants respectfully submit that the present application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

DINSMORE & SHOHL L.L.P.



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